FIG. 1A

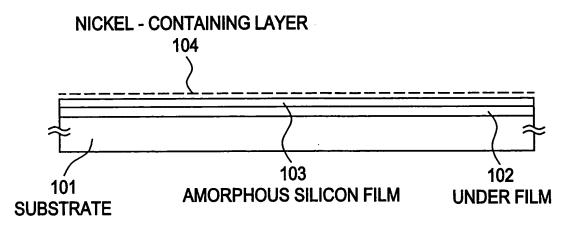


FIG. 1B

LASER CRYSTALLIZATION STEP

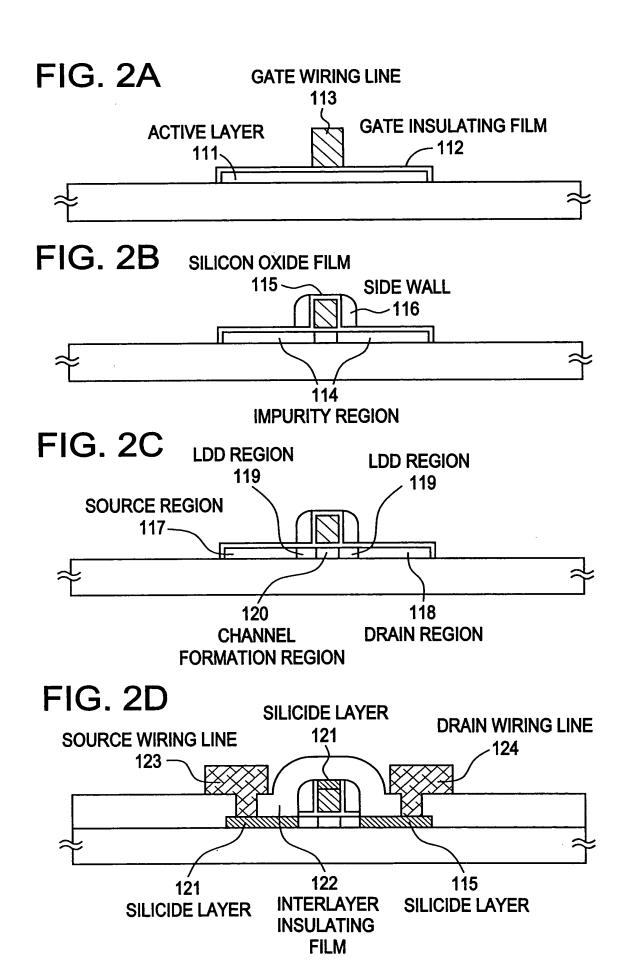
CRYSTALLINE SILICON FILM
105

FIG. 1C

THERMAL TREATMENT STEP IN REDUCING ATMOSPHERE

CRYSTALLINE SILICON FILM

106



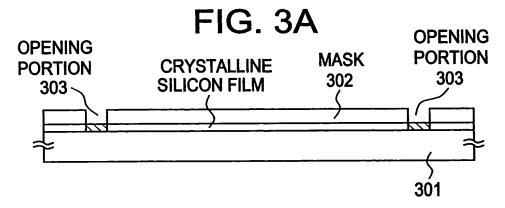


FIG. 3B

ADDING STEP OF PHOSPHORUS

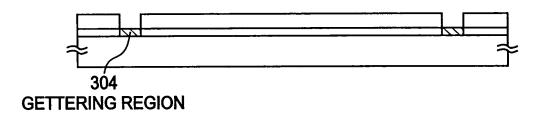


FIG. 3C

CRYSTALLINE SILICON FILM 305

FIG. 3D

HEAT TREATMENT STEP IN REDUCING ATMOSPHERE

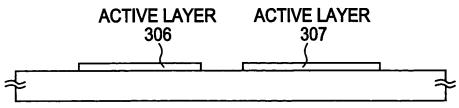


FIG. 4A

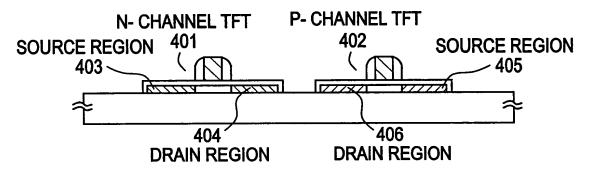
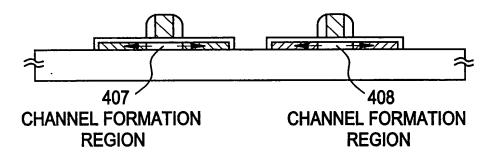
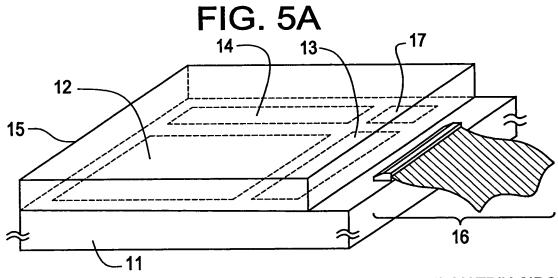


FIG. 4B GETTERING STEP



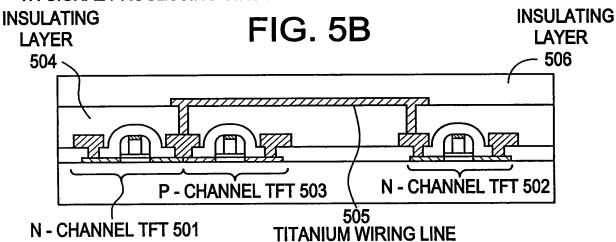


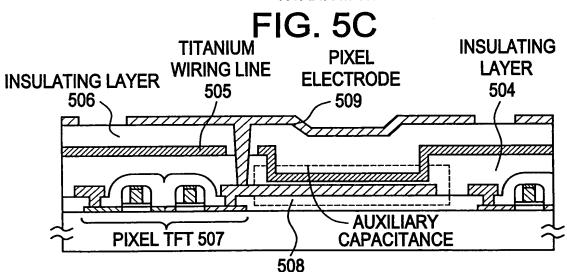
- 11: SUBSTRATE HAVING INSULATING SURFACE
- 13: SOURCE DRIVER CIRCUIT
- 15: OPPOSITE SUBSTRATE
- 17: SIGNAL PROCESSING CIRCUIT

12: PIXEL MATRIX CIRCUIT

14: GATE DRIVER CIRCUIT

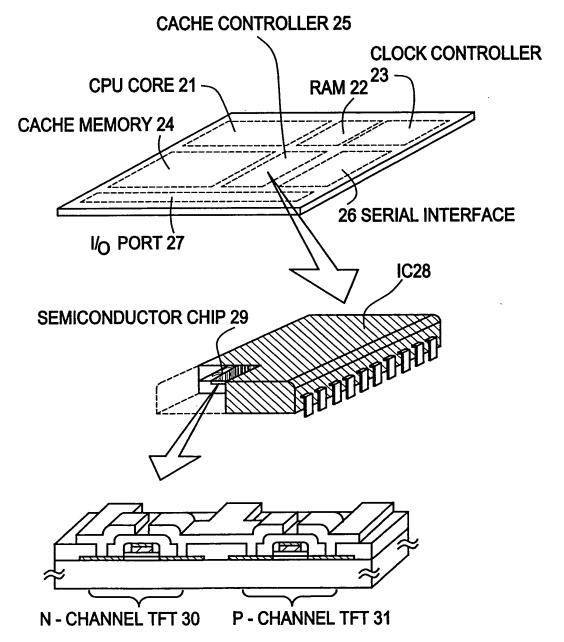
16: FPC

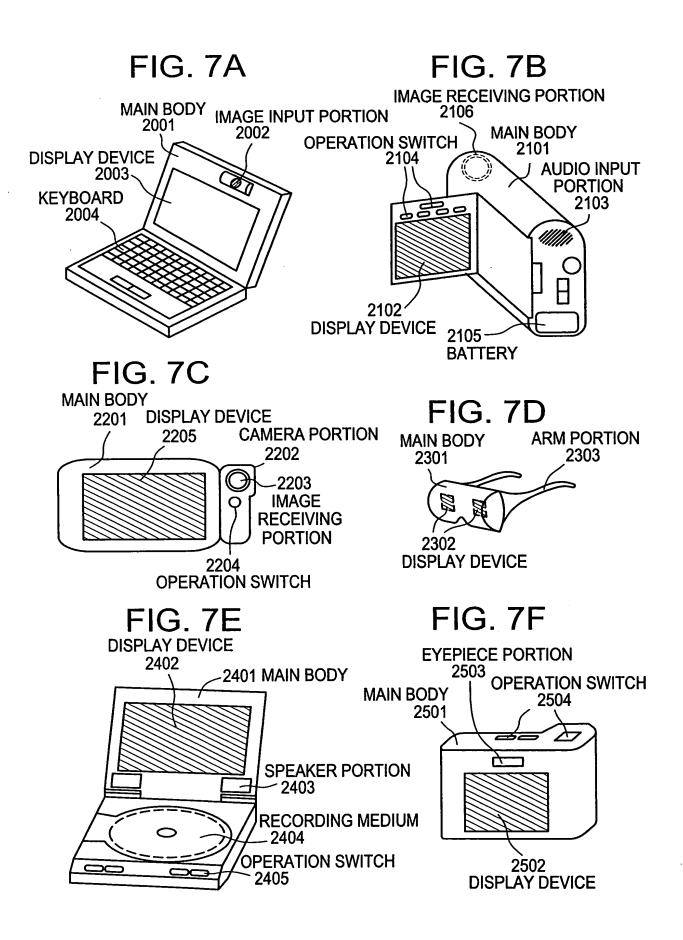




DRAIN WIRING LINE

FIG. 6





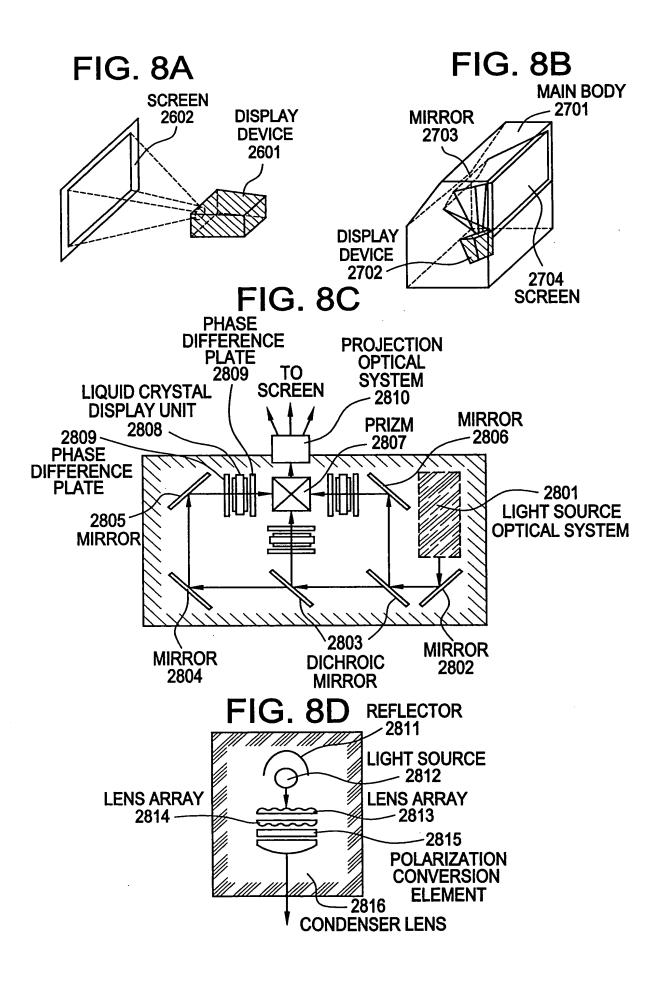


FIG. 9A

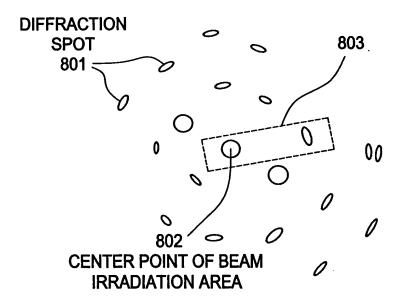


FIG. 9B

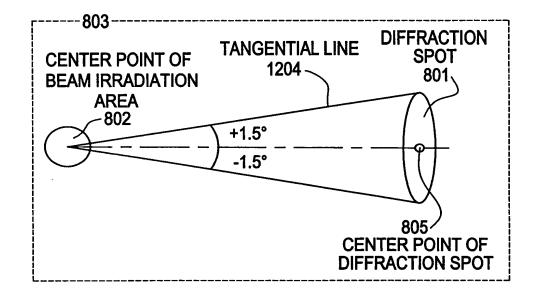


FIG. 10

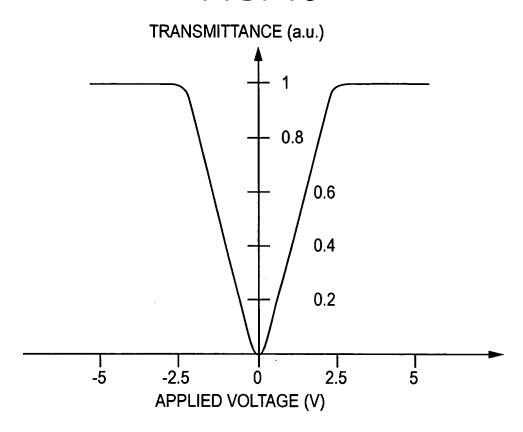
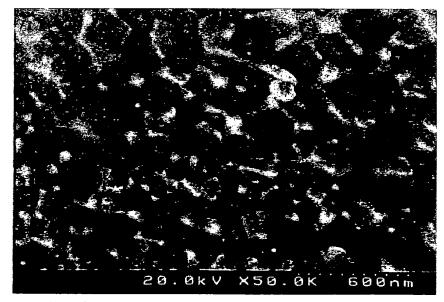
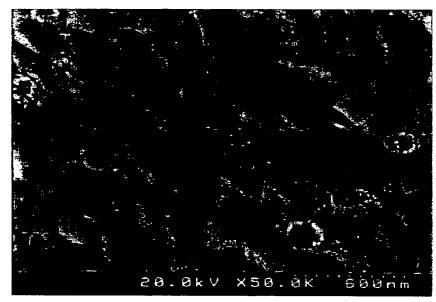


FIG. 11



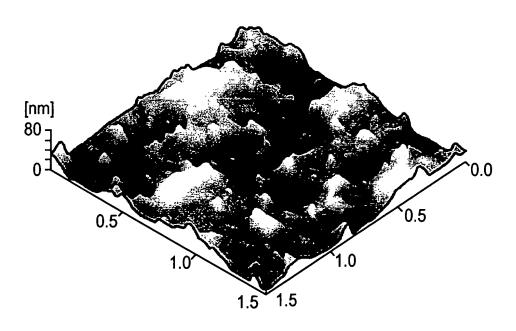
BEFORE HIGH TEMPERATURE ANNEALING

FIG. 12



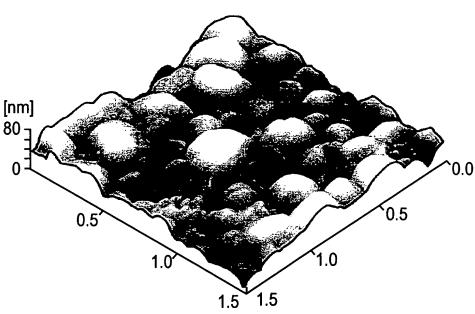
AFTER HIGH TEMPERATURE ANNEALING

FIG. 13



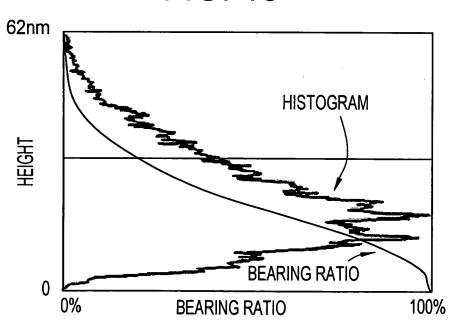
BEFORE HIGH TEMPERATURE ANNEALING

FIG. 14



AFTER HIGH TEMPERATURE ANNEALING

FIG. 15



BEFORE HIGH TEMPERATURE ANNEALING

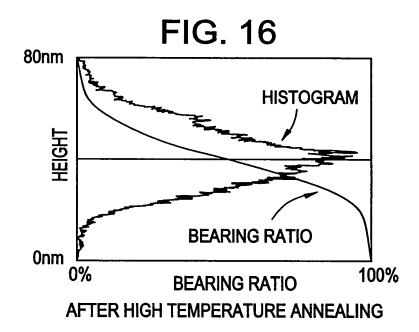


FIG. 17

OBSERVATION REGION	BEFORE HIGH TEMPERATURE ANNEALING	AFTER HIGH TEMPERATURE ANNEALING
1	13.623	40.925
2	20.027	51.126
3	20.629	59.364
4	21.798	48.539
5	16.666	55.341
6	15.097	46.510
7	13.120	57.655
8	14.035	51.120
9	12.599	54.416
10	20.699	36.945
MINIMUM (%)	12.60	36.95
MAXIMUM (%)	21.80	59.36
AVERAGE (%) VALUE	16.83	50.19
STANDARD DEVIATION	3.61	7.18

BEARING RATIO AT 2⁻¹(P-V VALUE) (%)